CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8) Applicant(s): Hathaway et al.			Docket No. BUR920010008US1
Serial No. 09/899,413	Filing Date July 5, 2001	Examiner Phan, Trong Q.	Group Art Unit 2818

Invention: **REDUCED PESSIMISM CLOCK TESTS FOR A TIMING ANALYSIS TOOL**

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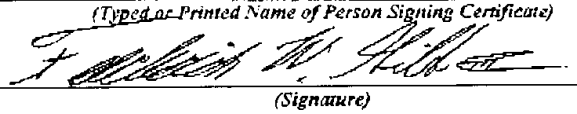

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Hathaway et al.

Serial No.: 09/899,413 Group Art Unit: 2818

Filing Date: July 5, 2001 Examiner: Phan, Trong Q.

For: REDUCED PESSIMISM CLOCK GATING TESTS FOR A TIMING ANALYSIS TOOL

Assistant Commissioner of Patents
Washington, D.C. 20231

AMENDMENT UNDER 37 CFR 1.111

IN THE SPECIFICATION:

Please substitute the following paragraph for the same numbered paragraph in the application.

[0049] Referring now to FIG. 10, a four-transistor (two p-type T_1, T_2, and two n-type T_3, T_4) gating device 26 is shown as an exemplary NAND clock gating device wherein the second embodiment of the invention as discussed above is implemented using EinsTimer using the methodology taught in U.S. Patent 5,508,937 discussed above. The relative sizes of the transistors is represented by the relative sizes of the transistor symbols T1-T4, showing that T2, which allow the gate signal to force or hold the output high, is smaller than the other transistors. This would cause the $delay_{gate}$ and $Slew_{gate}$ values for the falling gate input and rising gate output to be large, resulting in an unacceptably pessimistic clock gating setup requirement for this gate using the conventional propagated mode clock gating tests. As would be well known to those ordinarily skilled in the art the following reference signs shown in Figure 10 have the following meanings. The reference sign "clk" is an abbreviation for clock signal; a "gate" is a portion of a transistor; "slower (loaded)" means that the transistor in question has a load and is slower; the